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Development of Electroencephalography (EEG) Data Acquisition System based on FPGA PYNQ

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Abstract. This study proposed a novel Field Programmable Gate Array (FPGA)-based 32-channel data acquisition system to acquire and process Electroencephalography (EEG) signal. The data acquisition system utilized PYNQ-Z1 board, which was equipped with a Xilinx ZYNQ XC7Z020-1CLG400C All Programmable System-on-Chip (APSoCs) that offered high performance embedded system because of the combination between the flexibility and versatility of the programmable logic (PL) and the high-speed embedded processor or programmable system (PS). As the core of the data acquisition system, the FPGA collected, processed, and stored the data based on Front-End Analog to Digital Converter (ADC) ADS1299EEG-FE. The communication protocol used in the data acquisition system was Serial Peripheral Interface (SPI) with daisy-chain configuration. For the signal processing part, a 5th-order Butterworth bandpass filter and Fast Fourier Transform (FFT) has been implemented directly on the PYNQ's Overlay. The overlay was configurable FPGA design that extend the system from the PS of the ZYNQ to the PL, enabling us to control directly the hardware platform using Python running in the PS. The mean accuracy error obtained from validation result of the developed system was 1.34% and the Total Harmonic Distortion (THD) performance criterion resulting in 0.0091%, both of them validated with NETECH MiniSIM EEG Simulator 330. The comparison between the developed system and Neurostyle NS-EEG-D1 System acquiring the same EEG data shows correlation parameter gradient of 0.9818, y-intercept with -0.1803, and R squared of 0.9742 based on the least square analysis. The parameter above indicated that the developed system was adequate enough, if not on a par, with the commercialized, medical grade EEG data acquisition system Neurostyle NS-EEG-D1 as the system assured and maintained accuracy with higher sampling frequency.

Keywords: electroencephalography, data acquisition system, FPGA, PYNQ-Z1, ADS1299EEG-FE;

I. INTRODUCTION

Stroke is one of the leading causes of mortality and morbidity in both of developing and developed countries. It affects the quality of life of the survivor if it is not identified as early as possible from the onset of the stroke and followed with effective rehabilitation. Electroencephalography (EEG) can detect the disturbance caused by stroke by measuring the electrical activity of the brain generated by cooperative action of the brain cells. The amplitude of the electrical activity detected by EEG of a normal subject in the awake state, are within 10 to 100 μV and frequency with range from 0.5 to 45 Hz (Blinowska, 2006). EEG can be differentiated and analyzed based on the signal's frequency band, which is Delta (δ) (0.5 to 4 Hz), Theta (θ) (4 to 8 Hz), Alpha (α) (8 to 13 Hz), Beta (β) (13 to 30 Hz), and Gamma (γ) (above 30 Hz, usually to 45 Hz). There's already been documentation of abnormal EEG related to stroke in another studies (Bogousslavsky, 2003) (Naderi, 2010), where the conclusion of those study points that Quantitative EEG (qEEG) can be used to monitor and predict the progression and result of stroke rehabilitation (Finnigan, 2004).

Although there are already neuroimaging techniques that are capable to detect, identify, monitor, and predict stroke, the EEG is the longest one used to compare to the other. EEG have the closest approach to measuring the neural activity and temporal resolution that are broad and fast; EEG have spatial mapping capability that is the lowest compared to the other, but there are methods to overcome the spatial problems of EEG, such as LORETA or ICA. EEG can detect changes within a millisecond timeframe, compared to PET and fMRI that have time resolution between seconds and minutes. EEG measures the brain's electrical activity directly, while other methods record changes in blood flow (e.g., fMRI) or metabolic activity (e.g., PET), which are indirect markers of brain electrical activity. Furthermore, EEG has advantages in terms of budget, considering the

research boundary in Indonesia, and in terms of utilization and portability, hence the usage possibility of EEG is at the front line of stroke patients' brain management.

EEG is a measurement of potential difference; in the unipolar or referential configuration, it is measured relative to the same electrode for all the derivation. In contrast with the configuration of the electrode, there is a need of artefact rejection in EEG signal processing. The main problem lies in the definition of the main source or noise for an artefact, it can be generated from electromyography (EMG), electrocardiography (ECG), electrooculography (EOG), external magnetic field, loose electrode, the subject's movement, and from external factors such as power line interference at 50 to 60 Hz, depending on the region (Daly, 2012). All of the electrophysiological signal artefact above can be eliminated by recording them at the same time with the EEG but will need further filtering process to remove all of the remaining noise source.

This study was conducted to develop a data acquisition channel to acquire and process EEG signal. The data acquisition system utilized PYNQ-Z1 board based on Front-End Analog to Digital Converter (ADC) ADS1299EEG-FE. The communication protocol used in the data acquisition system was Serial Peripheral Interface (SPI) with daisy-chain configuration. The system was developed using all the 8-channel available in all of the four connected ADS1299EEG-FE in daisy-chain configuration, making the developed data acquisition system capable to acquire up to 32-channel, operating at data rate from 250 to 16 kSPS. Each of the channel has low noise, Programmable Gain Amplifier (PGA) and 24-bit Delta-Sigma ADC. For the signal processing part, a 5th-order Butterworth bandpass filter and Fast Fourier Transform (FFT) were implemented directly on the PYNQ-Z1's overlay. The overlay was configurable to FPGA design that extend the system from the Programmable System (PS) of the ZYNQ to the Programmable Logic (PL), enabling us to control directly the hardware platform using Python running in the PS and benefiting the capability of Python language in the signal processing part.

The paper was organized as follows. Section II presents the proposed architecture, design methodology, and system functionality. The results and discussions were presented in the Section III, while the conclusion was described in Section IV.

II. METHODS

Design of the Data Acquisition System

For the configuration of the data acquisition system, PGA modifier was set to 24 at 1000 SPS sampling rate. The data retrieval method was RDATA mode which can be used to read just one data output from the device (on-demand). The acquired data was then saved into the SD Card for signal processing and further analyses. The overview of the data acquisition system was shown in Figure 1.

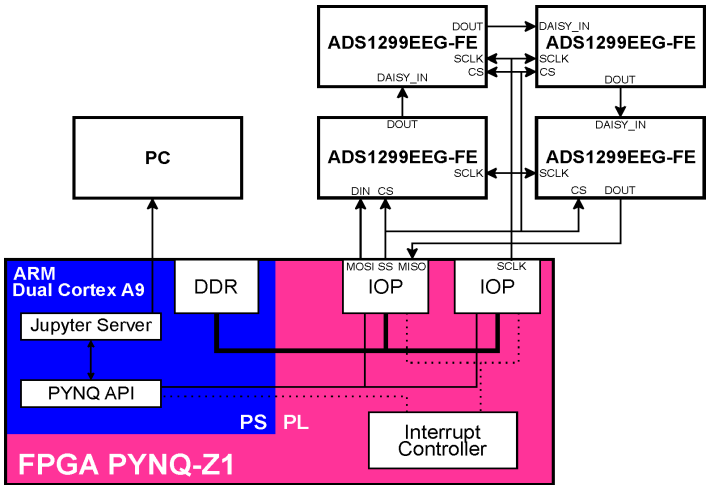


FIGURE 1. Design Scheme

The flowchart of the data acquisition system to acquire data from the ADS1299EEG-FE was shown in Figure 2. All the algorithm was implemented in C language and called by Python from the PS in the FPGA.

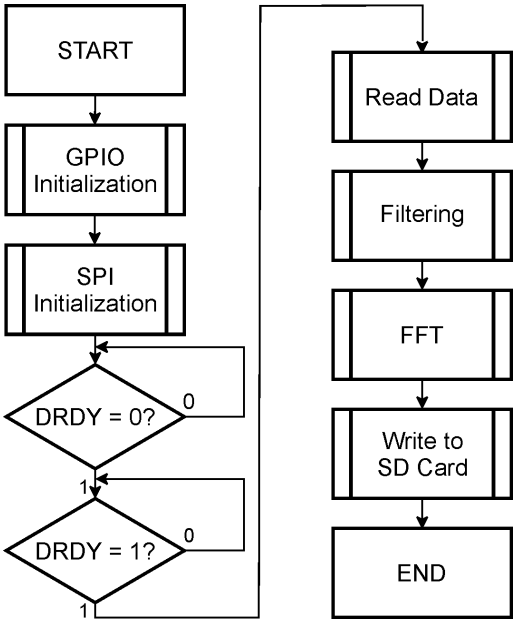


FIGURE 2. Flowchart of the developed system

For the verification of the developed data acquisition, there were numbers of method that were used which can be seen in Figure 3. The first thing to do was to acquire the resource utilization of the FPGA after the implementation of the designed architecture and the resource usage when the system is acquiring EEG data, which will be compared one to another for every data acquisition session. The resource utilization of the FPGA showed how much resource of the FPGA were used by the generated core.

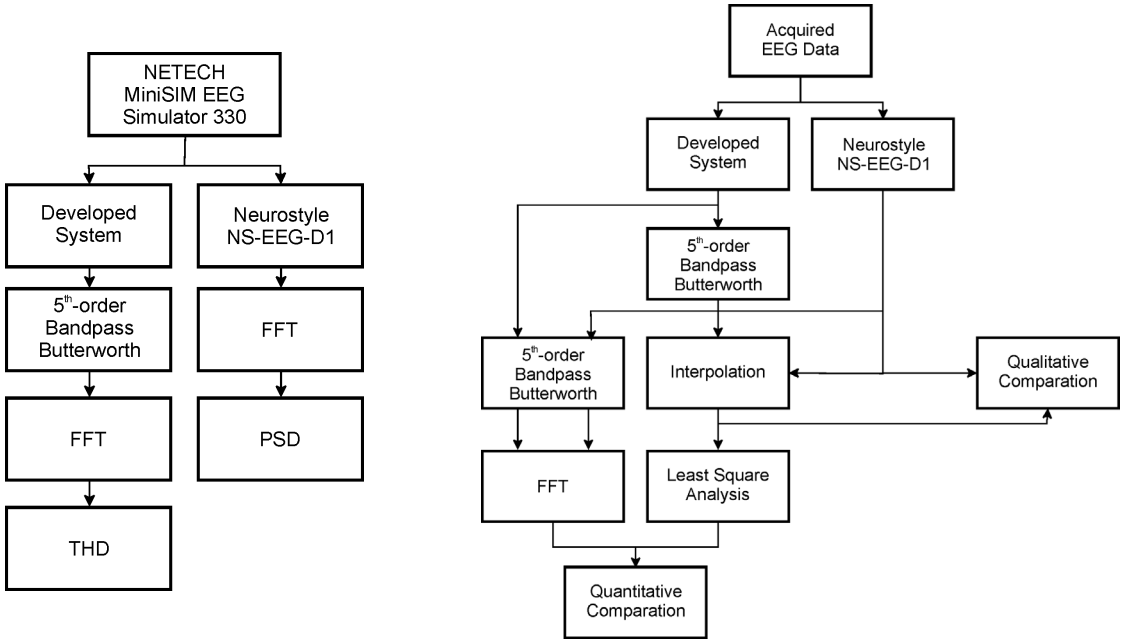
This study used NETECH MiniSIM EEG Simulator 330 for the second part, which will be used to simulate and determine the system's capability of measuring EEG signal, which was low in both frequency and amplitude. The variation for the frequency is 2 and 5 Hz with 10, 30, 50, and 100 μV difference in amplitude, where selection of the variation is based on the filter (bandpass from 0.5 to 50 Hz), hence all the frequency outside of the range will be attenuated. The data acquisition system was acquired at 20,000 sample with sampling frequency of 1000 SPS, as the duration of the acquisition time to 20 second.

After acquisition, digital filter was used to remove artefact or filter out the undesired signal from outside of the range of signal band frequency to minimize the noise in the output signal, hence the selection of the variation in simulation process. The filter type for the filtering process is 5th-order Butterworth bandpass filter. After filtering, V_{pp} could be calculated from each of the data amplitude. Statistical analysis was implemented with given algorithm below. Moreover, FFT was applied to the filtered signal to evaluate the dominance of the frequency and compared based on the configuration of each output of the NETECH MiniSIM EEG Simulator 330.

The processed signal, now in frequency domain, was further analyzed with Total Harmonic Distortion (THD). Both the filtering and FFT process were programmed in Python and implemented in the FPGA. THD was described as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency (Rebolledo-Herrerera, 2004). This performance criterion was used to evaluate harmonic distortion in the signal and as comparison based on the ADS1299 noise characteristics, according to the equation:

$$\mathrm{THD_F} = \frac{\sqrt{\sum_{n=2}^{\infty} A_{n\_rms}^2}}{A_{1\_rms}} \times 100\% \tag{2}$$

where A_{n_rms} is the root-mean-square amplitude of the nth harmonics and A_{1_rms} is the root-mean-square amplitude of the fundamental frequency.



(a) (b)

FIGURE 3. Block diagram for (a) validation method by simulation using NETECH MiniSIM EEG Simulator 330 and (b) comparison between the developed system and Neurostyle NS-EEG-D1 System

The last part of the method was to compare the real EEG measurement results from the developed data acquisition system with a commercialized, medical-grade EEG data acquisition system, which in this study is using Neurostyle NS-EEG-D1 System as the control. Before further method was applied, validation the Neurostyle NS-EEG-D1 System based on the same tool to validate the system was required, which is the NETECH MiniSIM EEG Simulator 330. The variation for this validation part was sinusoidal waveform with frequency from 0.1 and 5 Hz for each of amplitude: 10, 30, 50, 100, and 500 µV. Analysis of this validation part used Power Spectral Density (PSD) which generated amplitude spectrum with the real value only. Furthermore, the results of the previous work were normalized work against the range of the frequency bin to get $\mu V^2/Hz$ value, hence deprivation the dependency from bin range and evaluation the comparison of the level of the signal with different range could be done.

After the validation of the Neurostyle NS-EEG-D1 System, the next step was to compare both systems. Acquisition of the data used stackable jumper type JUMP100C that connected the head cap to both systems, for 15 minutes as the acquisition duration, resulted in 900,000 data sample with sampling frequency of 1000 SPS. Before comparing both systems, interpolation of the data acquired from the developed data acquisition system will be needed because there was a difference in sampling rate of both system (512 SPS for Neurostyle NS-EEG-D1 System and 1000 SPS for the developed data acquisition system). The interpolation method was linear, using loop to find the same index for each data from Neurostyle NS-EEG-D1 System and interpolation based on the same index for the developed data acquisition system. After the same data for each time based on the interpolation result calculated, the correlation graphs between the developed system and the Neurostyle NS-EEG-D1 System were then plotted and analyzed based on least square method.

III. RESULTS AND DISCUSSIONS

Resource Utilization and Resource Usage of the Data Acquisition System

The resource utilization did not contribute to the resource usage at all when the developed data acquisition system was running. The average of five session for the resource usage shows 72.47 ± 1.284 which was relatively high considering the implemented algorithm in the FPGA (5^{th}-order Butterworth bandpass filter, FFT, THD) and the need to implement Graphical User Interface (GUI) and post-processing method in the further study.

TABLE 1. Resource Utilization Report

Resource	Utilization	Available	Utilization (%)
LUT	36798	53200	69.17
LUTRAM	6372	17400	36.62
FF	41667	106400	39.16
BRAM	97.63	140	69.74
DSP	203	220	92.27

TABLE 2. Resource Usage Report

Trial	Resource Usage (%)
1	70.84
2	73.28
3	71.41
4	72.95
5	73.86
Average	72.47 ± 1.284

The developed system is utilizing a high portion of the Digital Signal Processing (DSP) block, and this is due to all the signal processing part in the system is implemented in the FPGA. The factor that may contribute largest to the high resource usage is due to the overhead of abstraction and complex layer of the Python language (high-level) compared to the C language (low-level) that can utilize direct memory management and statement directly following the clock cycle.

Simulation with NETECH MiniSIM EEG Simulator 330

As shown as in the Table 3, there are errors in the overall average, particularly for the low amplitude (10 μV) and other frequency peak for the 5 Hz frequency variation. There are some factors that may contribute to the error which this study has mitigated, such as:

- SPI communication protocol method, where the developed system used RDATA mode to retrieve data from the ADS1299 in on-demand mode by the developed data acquisition system. This method reduces the possibility of data loss.
- Implementation of signal processing in the system, which process the data accordingly to timing of the data acquisition, compared to RDATAC mode that may have caused data rate difference between input and output, hence the error.
- Power line interference, where the developed system already used DC power as to reduce this factor. Furthermore, the parameter of the filter is enough to eliminate the 50 Hz frequency from AC power line interference.
- Technical factors, such as checking the physical condition of each electrode, reducing the distance between the NETECH MiniSIM EEG Simulator 330 with the developed data acquisition system, and evaluating the contact impedance by utilizing the impedance testing feature from Neurostyle NS-EEG-D1 System.

Other than the factors mentioned above, this study examined the developed system further via THD analysis.

TABLE 3. Resume of the accuracy of the developed system

Variation		Average	
Frequency (Hz)	**Amplitude (µV)**	**Amplitude (µV)**	**Error (%)**
2	10	13.1	3.08
	30	30.6	1.02
	50	49.3	0.80
	100	99.8	0.59
5	10	12.9	2.95
	30	30.2	0.92
	50	49.4	0.76
	100	99.7	0.65

Total Harmonic Distortion (THD) Analysis

The harmonic distortion relative to an ideal sinusoidal waveform generated by NETECH MiniSIM EEG Simulator 330 is measured by THD analysis, based on equation (2). The results are shown in Table 3. Based on the datasheet, ADS1299EEG-FE have THD performance of -99 dB (with input voltage of -0.5 dBFs, input frequency of 10 Hz, gain equal to 12, and sampling rate of 250 SPS), hence the half of the ideal value of that ADS12999EEG-FE. Theoretically, the waveform generated by the NETECH MiniSIM EEG Simulator 330 has zero harmonic components, hence the closer the THD value to 0%, the fewer the distortion that exist in the measured signal. There is a main factor that may have contribute to both THD and the errors in the previous analysis. The power source that this study used acts as nonlinear load, which may generate distorted waveform that have harmonics. The unwanted distortion can add more current to the power system, which may cause high temperature and thermal residue on the measured signal. Moreover, harmonics with high frequency can interfere the communication transmission if there are oscillation between the high frequency and the communication frequency that are used (4 MHz).

TABLE 3. Resume of the THD analysis of the developed system

Variation		Average	
Frequency (Hz)	**Amplitude (µV)**	**THD (%)**	**THD (dB)**
2	10	0.0132	-38.00
	30	0.0111	-39.48
	50	0.0090	-41.39
	100	0.0097	-40.60
5	10	0.0084	-42.10
	30	0.0131	-38.73
	50	0.0125	-39.51
	100	0.0080	-43.72

Validation of Neurostyle NS-EEG-D1 System

The results from the validation of Neurostyle NS-EEG-D1 System by using NETECH MiniSIM EEG Simulator 330 can be seen in Figure 4. All the frequency with 0.1 Hz does not show the dominance of 0.1 Hz frequency, instead showing another frequency peak at approximately 25.5 Hz and power line interference at 50 Hz, although every possible source of power line interference has been replaced and using DC power for all of the connected device to Neurostyle NS-EEG-D1 System.

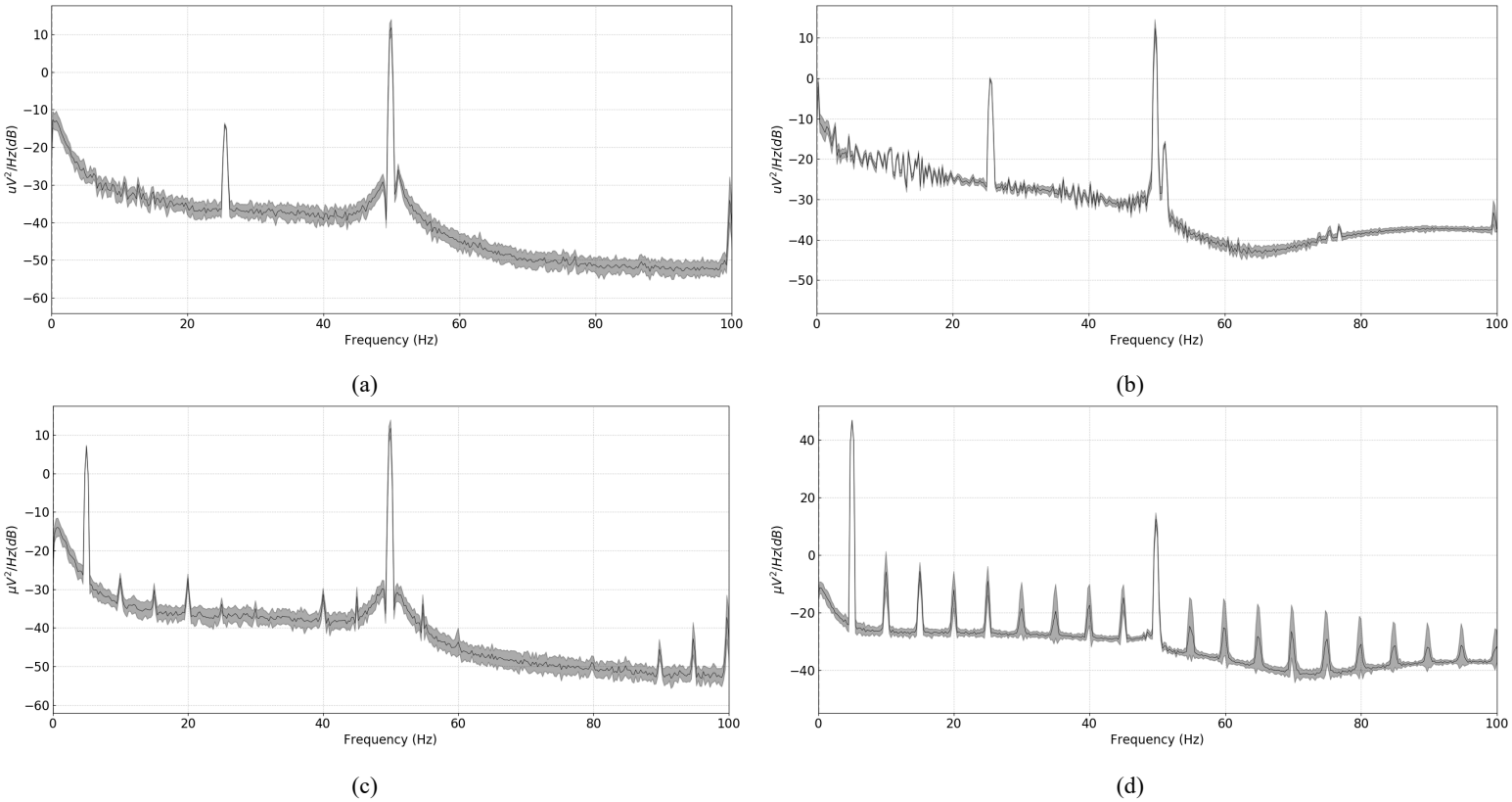


FIGURE 4. PSD analysis results example with variation of 0.1 Hz (a) 10 μV and (b) 500 μV, 5 Hz (c) 10 μV and (d) 500 μV

The results for 5 Hz variation in frequency shows that there is still power line interference, same as the results from 0.1 Hz frequency variation. Therefore, the data acquisition system will need filter to further eliminate this power line interference. Furthermore, the existence of harmonics in the 5 Hz results. All these data will be the basis for the next analysis, for further comparison with the developed data acquisition system.

Comparison with Neurostyle NS-EEG-D1 System

For the last part of the method, the parameter resulting from least square is presented in Table 4.

TABLE 4. Parameter of correlation

Parameter	Average	Standard Deviation
m	0.9818	0.0101
c (μV)	-0.1803	0.0048
R^2	0.9742	0.0124

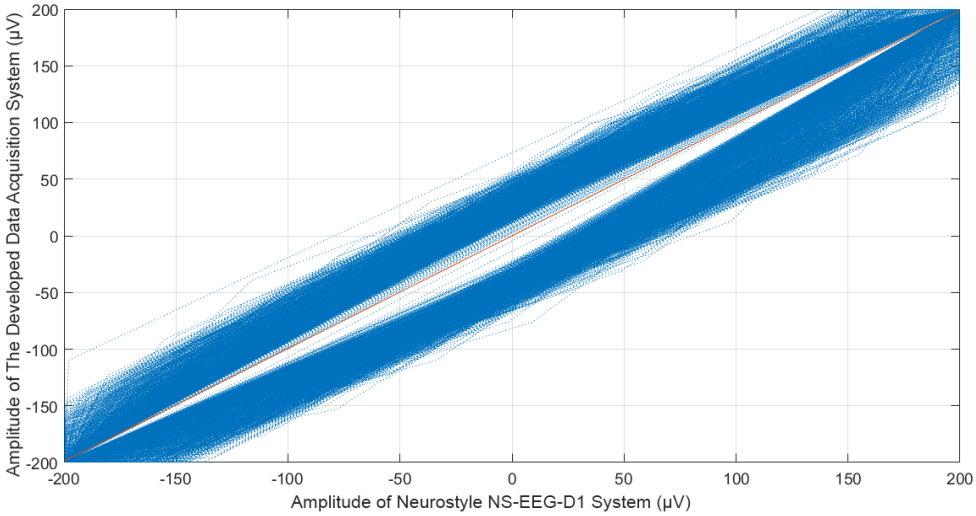


FIGURE 5. Correlation plot between the developed system and Neurostyle NS-EEG-D1 System example of one channel (O2)

It can be seen, in average, the change of the developed data acquisition system is concomitant with the change in the Neurostyle NS-EEG-D1 System and how the former will respond can be predicted accordingly, if the data for the latter system has been acquired before. All the parameter shows that both systems have linear correlation, hence the developed data acquisition system is on a par with the commercialized, medical-grade EEG data acquisition system. Moreover, from visual inspection within the Figure 6, the comparison based on difference between both systems shows insignificant error in the amplitude, compared to the maximum recorded amplitude.

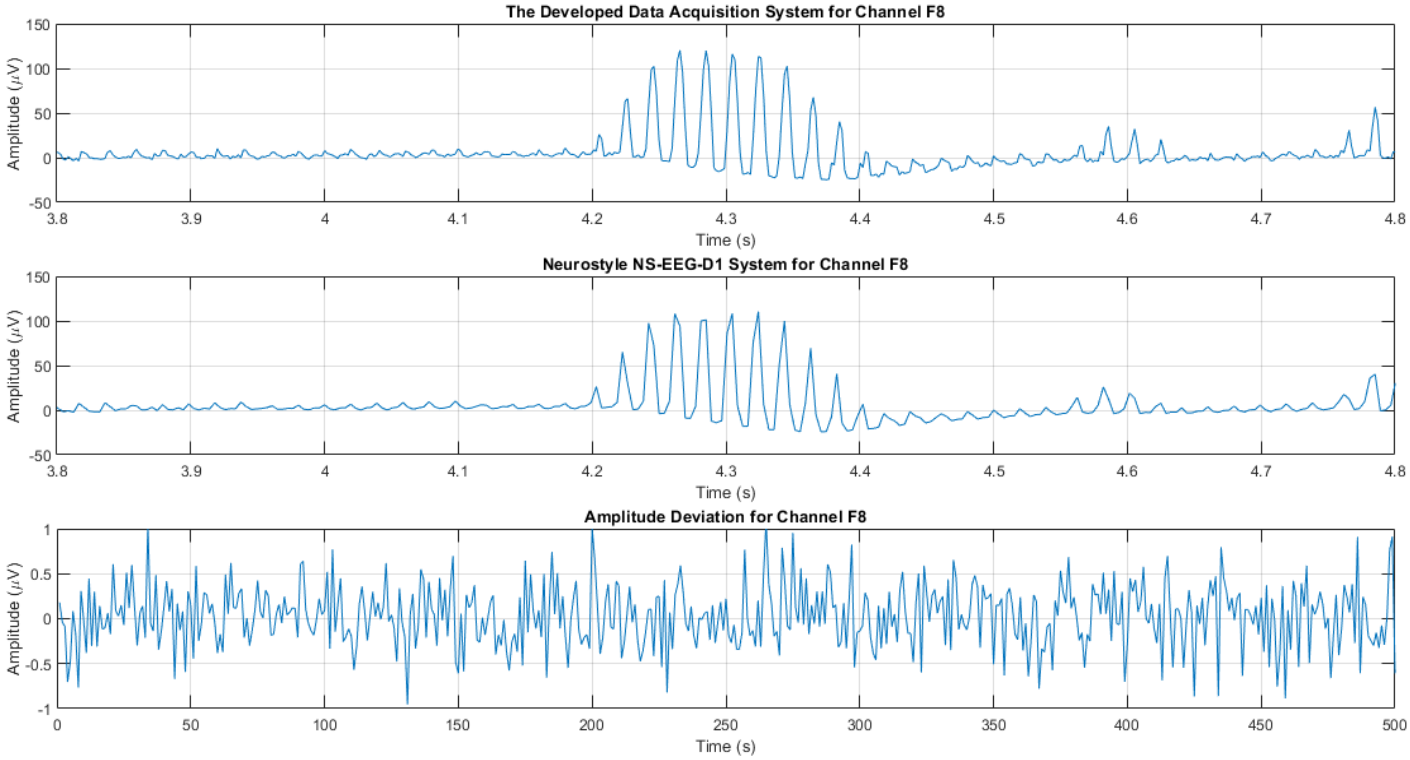


FIGURE 6. Visual qualitative comparison example of one channel (F8)

IV. CONCLUSION

A FPGA PYNQ-based 32-channel data acquisition system to acquire and process EEG signal has been built, utilizing the Front-End ADC ADS1299EEG-FE connected with SPI in daisy-chain configuration. For the signal processing part, a 5th-order Butterworth bandpass filter and Fast Fourier Transform (FFT) directly on the PYNQ's Overlay has been successfully implemented. The mean accuracy error obtained from validation result of the developed system is 1.34% and the Total Harmonic Distortion (THD) performance criterion resulting in 0.0091%, both validated with NETECH MiniSIM EEG Simulator 330. The comparison between the developed system and Neurostyle NS-EEG-D1 System acquiring the same EEG data shows correlation parameter gradient of 0.9818, y-intercept with -0.1803, and R squared of 0.9742 based on the least square analysis.

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